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**Code No: A5706**

**JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD**
**M.Tech I Semester Examinations, March/April-2011**
**CPLD AND FPGA ARCHITECTURE AND APPLICATIONS**
**(VLSI SYSTEM DESIGN)**

**Time: 3hours** **Max. Marks: 60**

**Answer any five questions**
**All questions carry equal marks**

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1. a) A circuit has four inputs RSTU and four outputs VWYZ. RSTU represents a binary coded decimal digit. VW represents the quotient and YZ represents the remainder when RSTU is divided by 3. Assume the invalid inputs do not occur. Realize the circuit using a ROM.
   b)With a neat sketch of MAX 5000 device macro cell. Explain how the sequential logic is implemented. [12]

2. a) What are the salient features of XC4000 FPGA CLB?
   b) What are the salient features of Altera's FLEX 8000 FPGA logic element? [12]

3. Design a Mealy sequential circuit using one-hot assignment which investigates an input sequence X and which will produce and output of Z = 1 for any input sequence ending in 1010. [12]

4. What are the features of the extended Petri Nets used for parallel controllers? [12]

5. How would you implement a Melay machine using a CPLD? [12]

6. How would you implement the function Y = A + B + C using Actel Act1 FPGA? [12]

7. How would you implement a binary counter using the CLBs of FPGA? [12]

8. Write a short notes on any **two** of the following:
   i) Altera FLEX logic - 1000 series CPLD
   ii) Cypress Flash 370 Device
   iii) 'AMD' CPLD. [12]

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